WHAT IS CLAIMED IS:

1. A data processor having a clustered architecture comprising:

a branching cluster and a non-branching cluster, each capable of computing branch conditions, said branching cluster operable to perform branch address computations for said branching cluster and said non-branching cluster; and

remote conditional branching control circuitry that causes said branching cluster to perform a branch address computation in response to sensing a conditional branch instruction in said non-branching cluster, and that communicates a computed branch condition from said non-branching cluster to said branching cluster.

2. The data processor as set forth in Claim 1 wherein each of said branching cluster and said non-branching cluster comprises at least one register file.

3. The data processor as set forth in Claim 1 wherein each of said branching cluster and said non-branching cluster comprises an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing at least one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline.

4. The data processor as set forth in Claim 1 wherein said remote conditional branching control circuitry further causes said branching cluster to perform a next program counter address computation in response to sensing a conditional branch instruction in said non-branching cluster.

5. The data processor as set forth in Claim 4 wherein said remote conditional branching control circuitry selects one of said computed next program counter address and said computed branch address in response to said computed branch condition.

6. The data processor as set forth in Claim 5 wherein said remote conditional branching control circuitry comprises a multiplexor that is responsive to said computed branch condition.

7. The data processor as set forth in Claim 1 wherein said data processor issues a shadow conditional branch instruction in said branching cluster to perform said branch address computation in response to sensing said conditional branch instruction in said non-branching cluster.

8. For use in a data processor comprising at least a branching cluster and a non-branching cluster, each capable of computing branch conditions, said branching cluster operable to perform branch address computations for said branching cluster and said non-branching cluster, a method of operating said data processor comprising the steps of:

computing a branch address in response to sensing a conditional branch instruction in said non-branching cluster; and

communicating a branch condition computed by said non-branching cluster from said non-branching cluster to said branching cluster.

9. The method of operating said data processor as set forth in Claim 8 further comprising the step of computing said branch condition in said non-branching cluster.

10. The method of operating said data processor as set forth in Claim 9 further comprising the step of computing a next program counter address.

11. The method of operating said data processor as set forth in Claim 10 further comprising the step of selecting one of said computed next program counter address and said computed branch address in response to said computed branch condition.

12. The method of operating said data processor as set forth in Claim 8 wherein each of said branching cluster and said non-branching cluster comprises an instruction execution pipeline comprising N processing stages, said method further comprising the step of performing in each of said N processing stages at least one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline.

13. The method of operating said data processor as set forth in Claim 8 further comprising the step of issuing a shadow conditional branch instruction in said branching cluster to perform said branch address computation in response to sensing said conditional branch instruction in said non-branching cluster.

14. A processing system comprising:

a data processor having a clustered architecture;

a memory associated with said data processor;

a plurality of peripheral circuits associated with said data processor for performing selected functions in association with said data processor, wherein said data processor comprises:

at least a branching cluster and a non-branching cluster that are capable of computing branch conditions, said branching cluster operable to perform branch address computations for said at least said branching cluster and said non-branching cluster; and

remote conditional branching control circuitry that causes said branching cluster to perform a branch address computation in response to sensing a conditional branch instruction in said non-branching cluster, and that communicates a computed branch condition from said non-branching cluster to said branching cluster.

15. The processing system as set forth in Claim 14 wherein each of said branching cluster and said non-branching cluster comprises at least one register file.

16. The processing system as set forth in Claim 14 wherein each of said at least said branching cluster and said non-branching cluster comprises an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing at least one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline.

17. The processing system as set forth in Claim 14 wherein said remote conditional branching control circuitry further causes said branching cluster to perform a next program counter address computation in response to sensing a conditional branch instruction in said non-branching cluster.

18. The processing system as set forth in Claim 17 wherein said remote conditional branching control circuitry selects one of said computed next program counter address and said computed branch address in response to said computed branch condition.

19. The processing system as set forth in Claim 18 wherein said remote conditional branching control circuitry comprises a multiplexor having an input channel associated with said non-branching cluster, said multiplexor responsive to said computed branch condition.

20. The processing system as set forth in Claim 14 wherein said data processor issues a shadow conditional branch instruction in said branching cluster to perform said branch address computation in response to sensing said conditional branch instruction in said non-branching cluster.